REMARKS

Claims 1-19 are pending in the Application. Claim 19 is canceled.

Claims 1, 8 and 14 have been amended to clearly recite that the metal layer being electroplated at least substantially fills the apertures. Support for this is found throughout the Application, such as at page 10, lines 7-8, page 17, lines 26-27, page 18, lines 8-9 and 22-23, and page 19, lines 27-28. Also, claims 1, 8 and 14 have been amended to recite the steps of electroplating substantially filling apertures with metal on electronic devices when a first electronic device has been found to have substantially filled apertures having voids. Such amendment is supported by the claims as originally filed. Claims 5 and 11 have been amended only to insert the missing conjunction --and-- and not to overcome any prior art rejection. No new matter is added with this Amendment.

Fig. 1 has been amended to include the legend --Prior Art--. Applicant respectfully requests that the objection to Fig. 1 be withdrawn.

Claims 1 and 12 have been objected to because of typographical errors, which errors have been corrected by the present Amendment. Applicant respectfully requests that these objections be withdrawn.

Claims 1, 2 and 14 have been rejected under 35 USC § 102(b) as being anticipated by Sakamoto et al. (US 5,788,830). Applicant respectfully traverses.

Applicant's invention is directed to a method of electroplating a layer of metal on electronic devices having a copper containing seed layer and apertures, where the apertures are at least substantially filled with the metal, when a first electronic device has been found to have voids in apertures that are at least substantially filled with metal

The Sakamoto patent does not disclose substantially filling apertures (through holes) as required by Applicant's claims. In fact, this patent is quite clear that only the *inner walls* of the through holes are plated with copper. See, e.g., column 5, lines 51-53 (". . . it can produce evenly attached and highly reliable electroplating even on the *internal walls* of through-holes. . ."

[Emphasis added]) and column 6, line 66 to column 7, line 1 ("This electroplating process using the palladium compound is suitably applied to electroplating the *inner walls* of through-holes of printed wiring boards." [Emphasis added]). Applicant submits that the Sakamoto patent does not anticipate the presently claimed invention and respectfully requests that this rejection be withdrawn.

Claims 1-5, 7-11, 13-16, 18 and 19 have been rejected under 35 USC § 103(a) as being unpatentable over EP 1 005 078 in view of either Sakamoto or Carano et al. (US 6,375,731).

As discussed above, Applicant's invention is directed to a method of electroplating a layer of metal on electronic devices having a copper containing seed layer and apertures, where the apertures are at least substantially filled with the metal, when a first electronic device has been found to have voids in apertures that are at least substantially filled with metal. Applicant's claims require that a first electronic substrate have voids in substantially metal-filled apertures, where such apertures also have a copper-containing seed layer.

As stated in the Official Action at page 6, EP '078 discloses a method that does not create voids, and thus seed layer repair steps are not necessary. Nothing in this patent teaches or suggests how to repair seed layers after voids have been found in apertures that are at least substantially filled with electrodeposited metal.

As discussed above, the Sakamoto patent fails to teach or suggest apertures that are at least substantially filled with metal. Further, nothing in this reference discloses or suggests repairing copper-containing seed layers.

The Carano patent discloses treating a non-conductive substrate with certain cleaners/conditioners prior to depositing a conductive carbon composition. Copper is subsequently electroplated on the conductive carbon composition. This patent neither teaches nor suggests copper-containing seed layers. Further, this patent teaches that by using the certain cleaners/conditioners *prior* to the deposition of the conductive carbon composition that void formation is prevented. Thus, nothing in this patent teaches or suggests how to *repair* a copper-containing seed layer after voids are found. Still further, this patent clearly teaches that through holes are <u>not</u> filled by electroplating metal. See column 1, lines 47-48, which clearly states that a

properly soldered through hole is filled with solder", thus such through hole cannot be filled with electroplated metal. Thus, nothing in the Cerano patent teaches or suggests electroplating a layer of metal to at least substantially fill apertures in the device.

One skilled in the art looking to repair copper-containing seed layers in apertures that are subsequently at least substantially filled with electrodeposited metal would not look to either Sakamoto or Cerano, as neither of these references discloses substantially filling apertures or repairing problems in the copper-containing seed layers. Even if one did combine either Sakamoto or Cerano with EP '078, there is nothing in these combinations that teaches or suggests the presently claimed invention. Applicant submits that the Examiner has not made out a prima facie case of obviousness and respectfully requests that this rejection be withdrawn.

.Claims 6, 12 and 17 have been rejected under 35 USC § 103(a) as being unpatentable over EP 1 005 078 in view of either Sakamoto or Carano, and further in view of either Reid (US 6,024,857) or Andricacos et al. (US 6,395,164).

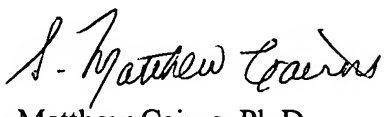
EP '078, Sakamoto and Carano are discussed above, alone and in combination.

The Reid patent is relied on for teaching certain aspect ratios and dimensions of apertures. However, this patent does not fill the deficiencies of EP '078, Sakamoto and Carano, alone or in any combination. Reid is directed to filling apertures with copper without voids. Reid neither discloses nor suggests the use of a copper-containing seed layer. In fact, Reid is completely silent on the presence of a seed layer. One skilled in the art looking to manufacture electronic device having copper-containing seed layers would not look to the Reid patent as seed layers are not present in this disclosure. Applicant submits that there is no motivation to combine Reid with any of EP '078, Sakamoto and Carano. Even if one does combine Reid with any of EP '078, Sakamoto and Carano, nothing in Reid teaches or suggests Applicant's claimed process.

The Andicacos patent is also relied on for teaching certain aspect ratios and dimensions of apertures. Nothing in this patent teaches or suggests how to repair seed layers after voids have been found in apertures that are at least substantially filled with electrodeposited metal. Thus, this patent does not fill the deficiencies of EP '078, Sakamoto and Carano, alone or in any combination.

Applicants respectfully request favorable reconsideration in the form of a notice of allowance.

Respectfully submitted,



S. Matthew Cairns, Ph.D.
Attorney for Applicant
Registration No. 42,378

EDWARDS & ANGELL LLP
PO Box 55874
Boston, MA 02205
Date: June 2, 2004